ABSTRACT OF THE DISCLOSURE

An integrated circuit is provided that includes an execution engine and a memory controller. The execution engine is clocked at a first rate and the memory controller is clocked at a second rate that is less than the first rate. Pins on the integrated circuit can transfer data to and from the integrated circuit on both the rising and falling edges of a second clock transitioning at the second clock rate. The integrated circuit is preferably packaged using a lead frame and wire bonds extending from pads on the integrated circuit to corresponding leads. The leads are secured to trace conductors on a surface of a printed circuit board. The board contains no more than two conductive layers separated by a dielectric layer. Thus, an overall electronic system is formed having a board with no more than two conductive layers, an execution engine that receives a first clock signal, a memory controller which receives a second clock signal, and a memory device that sends data to and from the memory controller at twice the rate of the second clock signal. Using a throttled second clock signal allows for less expensive packaging and mounting of packaged integrated circuits on a less expensive PCB, while still maintaining use of a DDR DRAM transfer mechanism.